REMARKS

Claims 1-15 were presented for examination and were pending in this application. In an Official Action dated November 4, 2003, claims 1-15 were rejected. Applicants thank Examiner for examination of the claims pending in this application and addresses Examiner's comments below.

Applicants herein amend claim 1. Claim 16 is added. These changes are believed not to introduce new matter, and their entry is respectfully requested. The claims have been amended to expedite the prosecution of the application in a manner consistent with the Patent Office Business Goals, 65 Fed. Reg. 54603 (Sept. 8, 2000). In making these amendments, Applicants have not and do not narrow the scope of the protection to which Applicants consider the claimed invention to be entitled and do not concede that the subject matter of such claims was in fact disclosed or taught by the cited prior art. Rather, Applicants reserve the right to pursue such protection at a later point in time and merely seek to pursue protection for the subject matter presented in this submission.

Based on the above Amendment and the following Remarks, Applicants respectfully request that Examiner reconsider all outstanding objections and rejections, and withdraw them.

Response to Objections to the Specification

The Examiner has objected to the title as not being descriptive of the invention to which the claims are directed. Applicants have amended the title to correct the informalities noted by the Examiner. In particular, as amended the title indicates that "instruction level multithreading" of the present invention is in an "embedded processor" and uses "zero-time

context switching." These are features that distinguish the present invention from conventional multithreading schemes.

In addition, the Examiner has objected to the specification urging Applicants to review it and submit corrections for all mistakes of a grammatical, clerical, or typographical nature. Applicants have amended the specification in an effort to comply with Examiner's request by submitting several typographical and grammatical corrections. Now new matter has been entered.

Accordingly, Applicants respectfully request that Examiner reconsider and withdraw the objections to the specification and title.

Response to Rejection Under 35 USC 102(b)

In the 4th paragraph of the Office Action, Examiner rejects claims 1-3, 5-9, and 13-15 under 35 USC § 102(b) as allegedly being anticipated by U.S. Patent No. 6,317,774 to Jones et al. ("Jones"). This rejection is now traversed.

Claim 1, as amended, recites:

> A computer based system for switching between program contexts comprising:
>
> an embedded pipelined processor capable of having a first program thread and a second program thread in an execution pipeline;
>
> a first set of data storage devices capable of storing a first state of said embedded processor;
>
> a second set of data storage devices capable of storing a second state of said embedded processor; and
>
> a thread scheduler for identifying which of said program threads said embedded processor executes and configurable to allocate available processing time of the embedded pipelined processor among at least the first and second states according to a fixed schedule;
>
> wherein said processor switches between said first and second state after the end of the execution of a first program

instruction in the first thread and before the beginning of the execution of a second program instruction.

The claimed system includes an embedded pipeline processor capable of having at least two program threads in a pipeline and a thread scheduler that is configurable to allocate the processing time of the embedded processor according to a fixed schedule. Further, the embedded processor switches states of the threads in between the execution of two instructions, that is, in a zero-time manner thereby increasing computing speed. The fixed schedule is used to allocate computing time, for example quanta, which for example provides a guaranteed timely processing of hard-real-time processes.

In contrast, Jones simply describes a multithreading operating system scheduling feature using a directed acyclic graph of nodes (col. 2, lines 51-54). The scheduler of Jones "also supports embedded constrains, and the inheritance of constrains from threads blocked on a synchronization mechanism to the thread owning the synchronization mechanism." (col. 4, lines 49-52). Constrains as used in the Jones specification refers to a thread's "time constrains specifying that it needs a certain amount of processor time by a certain deadline." (col. 1, lines 59-61). As described in Jones, embedded constrains are constrains within constrains, that is, "a thread for which a constraint is already pending may submit a further constraint, called a 'nested constraint'." No other use of the term embedded constrain is described in Jones.

Therefore, Jones does not describe an embedded processor as recited in claim 1. Rather, Jones describes an operating system scheduling software that supports embedded or nested time constrains.

In a rejection under 35 U.S.C. §102, each and every claim element must be present in the applied reference. However, Examiner has failed to point out any prior "embedded pipeline processor" in Jones. Therefore, it is respectfully submitted that the rejection of claim 1 is improper and should be withdrawn.

As claims 2-15 are directly or indirectly dependent on claim 1, all arguments advanced above with respect to claim 1 are hereby incorporated so as to apply to claims 2-15.

Based on the above Amendment and Remarks, Applicants respectfully submit that for at least these reasons claims 1-3, 5-9, and 13-15 are patentably distinguishable over the cited reference. Therefore, Applicants respectfully request that Examiner reconsider the rejection, and withdraw it.

Response to Rejections Under 35 USC 103(a)

In the 16th paragraph of the Office Action, Examiner rejects claim 4 under 35 USC § 103(a) as allegedly being unpatentable over Jones in view of U.S. Patent No. 6,567,839 to Borkenhagen et al. ("Borkenhagen"). This rejection is respectfully traversed.

Applicants respectfully assert that the combination suggested by the Examiner's rejection under 35 U.S.C. § 103 is improper. It is well settled law that when making a rejection under 35 U.S.C. § 103, Examiner has the burden of establishing a prima facie case of obviousness. Examiner can satisfy this burden "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references" in the manner suggested by Examiner. In re Fine, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). "[E]lements of separate prior patents [and/or publications] cannot be combined when there is no suggestion of such combination anywhere in those patents [and/or publications]...; and a court should

avoid hindsight..." (emphasis added; annotations within square brackets). Panduit Corp. v. Dennison Mfg. Co., 1 USPQ2d 1593, 1597 (Fed. Cir. 1987), citing ACS Hospital Systems, Inc. v. Montefiore Hospital, 220 USPQ 929, 933 (Fed. Cir. 1984), and W.L. Gore & Associates v. Garlock, Inc., 220 USPQ 303, 313 (Fed. Cir. 1983). See also Uniroyal Inc. v. Rudkin-Wiley Corp., 5 USPQ2d 1434, 1438-1441 (Fed. Cir. 1988). In fact, it is impermissible to use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. In re Fine, 5 USPQ2d at 1600.

In particular, Examiner argues that because the Jones reference does not disclose the details of the mechanism to control the thread switch one of ordinary skill in the art would have been motivated to combine that system with the thread switch control register in Borkenhagen. However, Jones does disclose a method by which threads are switched, for example:

> A thread is typically represented by a data structure called an execution context ... When the operating system suspends a thread in favor of the execution of another thread, it copies the information from the registers and stack to the thread's execution context. When the operating system subsequently reselects the thread for execution after suspending another thread, it copies the information in the thread's execution context back to the actual registers and stack.

(Jones: col. 1, lines 19-30).

In addition, Jones teaches away from the combination with Borkenhagen to come up with the claimed invention because as Borkenhagen describes, it relates to a different multithreading:

> The term "multithreading" as defined in the computer architecture community is not the same as the software use of the term which means one task subdivided into multiple related

> threads. In the architecture definition, the threads may be independent. Therefore "hardware multithreading" is often used to distinguish the two uses of the term. Within the context of the present invention, the term multithreading connotes hardware multithreading to tolerate memory latency.

(Borkenhagen: col. 3, line 63-col.4, line 4). This is inconsistent with the description in Jones based on the operating system's multithreading capability and would lead one of ordinary skill in a direction divergent from the claimed invention. Accordingly, Jones teaches away from the claimed invention and cannot be properly used as a reference rejecting the present claims since by teaching away it does not provide any teaching or suggestion to combine. In re Gurley, 31 USPQ 1130, 31 (Fed. Cir. 1994). *See also*, In re Fine, 5 USPQ2d 1596, 1598-99 (Fed. Cir. 1988). "[E]lements of separate prior patents [and/or publications] cannot be combined when there is no suggestion of such combination anywhere in those patents [and/or publications]...; and a court should avoid hindsight....Likewise, the teaching of [the cited references] are inconsistent with the claimed invention" (emphasis added; annotations within square brackets). Panduit Corp. v. Dennison Mfg. Co., 1 USPQ2d 1593, 1597 (Fed. Cir. 1987), citing ACS Hospital Systems, Inc. v. Montefiore Hospital, 220 USPQ 929, 933 (Fed. Cir. 1984).

Even if, *arguendo*, the references could be combined, the result would still not constitute the claimed invention. Specifically, the context switching mechanisms described in the cited references do not describe "a thread scheduler ... configurable to allocate available processing time of the embedded pipelined processor among at least the first and second states according to a fixed schedule and wherein said processor switches between said first and second state after the end of the execution of a first program instruction in the first thread and before the beginning of the execution of a second program instruction" as recited

in claim 1. For example, the scheduling in Jones is based on a "acyclic graph of nodes" (col. 2, line 52), while the scheduling in Borkenhagen is based on events, such as latency events, and thread switch logic to determine based on the events whether to switch and to which thread (Borkenhagen: col. 12, lines 31-61).

Based on the above Amendment and Remarks, Applicants respectfully submit that for at least these reasons claim 4 is patentably distinguishable over the cited references, both alone and in combination. Therefore, Applicants respectfully request that Examiner reconsider the rejection, and withdraw it.

In the 18th paragraph of the Office Action, Examiner rejects claim 10-12 under 35 USC § 103(a) as allegedly being unpatentable over Jones in view of U.S. Patent No. 6,026,503 to Gutgold et al. ("Gutgold"). This rejection is respectfully traversed.

As described above with reference to claim 1, Jones fails to disclose at least "an embedded pipelined processor capable of having a first program thread and a second program thread in an execution pipeline." As claims 10-12 are dependent on claim 1 , all arguments advanced above with respect to claim 1 are hereby incorporated so as to apply to claims 10-12.

Further, Gutgold also fails to disclose as least this element. Gutgold describes a "device and method foe interactively debugging a system controlled by a microprocessor." (Abstract). Gutgold teaches the connection of a debugging device to a microprocessor/bus interface to monitor the exchange of signals. (col. 3, lines 20-22). There is no mention or suggestion of "an embedded pipelined processor" as claimed in the present invention.

Therefore, based on the above Amendment and Remarks, Applicants respectfully submit that for at least these reasons claims 10-12 are patentably distinguishable over the

cited references, both alone and in combination. Therefore, Applicants respectfully request that Examiner reconsider the rejection, and withdraw it.

Conclusion

Applicants have added new claim 16 for which Applicants request consideration and examination. Applicants respectfully submit that this claim is supported by the specification and is commensurate within the scope of protection to which Applicants believe they are entitled.

In sum, Applicants respectfully submit that claims 1 through 16, as presented herein, are patentably distinguishable over the cited references (including references cited, but not applied). Therefore, Applicants request reconsideration of the basis for the rejections to these claims and request allowance of them.

In addition, Applicants respectfully invite Examiner to contact Applicants' representative at the number provided below if Examiner believes it will help expedite furtherance of this application.

Respectfully Submitted,
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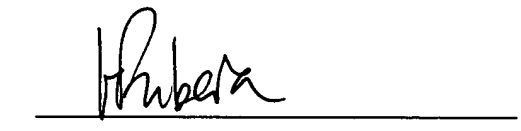
Date: Feb. 4, 2004 By: 

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